SEMICONDUCTOR PACKAGE ASSEMBLY AND METHOD FOR ELECTRICALLY ISOLATING MODULES

TECHNICAL FIELD

The present invention relates to semiconductor device packaging, and more particularly, to electrically isolating semiconductors within a package assembly.

BACKGROUND OF THE INVENTION

Computers are routinely used to receive and process data from peripheral devices such as digital cameras and digital video recorders. The peripheral devices typically transfer data to a computer via a serial bus. Viewing images captured by these peripheral devices in real-time, for example, requires the peripheral device to transfer a relatively large amount of data to the computer in a relatively short amount of time. In the past, computers used a Universal Serial Bus ("USB") to transfer such data, but a USB cannot guarantee real-time viewing of digital transmissions due to its inherent limitations. Thus, the IEEE 1394 standard was developed to allow simple, low-cost, high-bandwidth, real-time data interfacing between computers and peripherals without significant signal degradation.

IEEE 1394 is a nonproprietary, high-speed, serial bus input/output standard. It provides a comprehensive standard for connecting digital devices, including personal computers and consumer electronics hardware. It is also platform-independent, scalable (expandable), and flexible in supporting peer-to-peer (roughly, device-to-device) connections. IEEE 1394 preserves data integrity by eliminating the need to convert digital signals into analog signals. Created for desktop networks by Apple Computer, which called the technology FIREWIRE™, and further developed by the IEEE 1394 working group, it is considered a low-cost interface for devices such as digital cameras, camcorders, and multimedia devices. In addition, it is seen as a means of integrating personal computers and home electronics equipment.

Figure 1 illustrates peer-to-peer connections according to the IEEE 1394 standard. A computer 102 in a room 104 is communicatively coupled to a computer 106 in a room 108 via a serial bus 105. Another serial bus 109 is used to

communicatively couple the computer 106 to another computer 110 in another room 112. Each computer on the network includes networking components that implement IEEE 1394.

Figure 2 illustrates the IEEE 1394 networking components 200 that include a physical layer chip ("PHY") 202 and a link layer chip ("LINK") 204. The LINK chip 204 contains the networking intelligence to process and generate networking signals, such as arbitration signals and packets. The PHY chip 202 is the physical interface by which the computer system may receive or send networking information to and from the serial bus. The PHY chip 202 also serializes the data from the LINK chip 204 if the data is to be sent out to the serial bus 220, and likewise deserializes the data from the cable to be sent to the LINK chip 204 in parallel format. There are typically at least fourteen wires that communicatively couple the PHY chip 202 to the LINK chip 204.

IEEE 1394 specifies that all devices connected to a serial bus have the same reference ground potential as provided by the ground wire of the serial bus. IEEE 1394 recognizes, however, that separate devices connected to the bus may have different ground potentials. Such voltage differences could result in direct current flowing from the device having the higher ground potential to the device having the lower ground potential. Not only could such a current flow cause signal degradation, but it could cause damage to circuitry within the device as well. Thus, IEEE 1394 recommends that the ground wire of the serial bus be electrically isolated from the rest of the networking components in order that all PHY chips connected to a serial bus operate on the same isolated ground domain.

Figure 2 illustrates the recommended arrangement for electrical isolation of the PHY 202 and LINK 204 networking components. The ground 216 of the LINK chip 204 is coupled to the computer's chassis (not shown) as a reference. The ground 212 of the PHY chip is coupled to the ground 213 of the serial bus 220. A parallel configuration of a capacitor 208 and a resistor 206 effectively isolate the ground 213 of the serial bus 220 from the ground 216 of the LINK chip 204. The PHY and LINK chips are communicatively coupled by capacitors $214_{1\text{-}14}$.

This approach works well, but it is incompatible with the trend to reduce the size of electronic devices. Two major reasons account for the desire to decrease the size, shape, and configuration of electronic devices. First, smaller footprint circuitry allows a reduction in the trace lines that go from any pin on an integrated circuit package to the pad on a die, helping to increase signal integrity. Second, smaller components occupy less space on a printed circuit board, thus allowing more room for other useful components on the same printed circuit board. Hence, the solution offered by IEEE 1394 using an external capacitor and resistor to electrically isolate the PHY and LINK chips creates unnecessary bulkiness through use of additional electronic components. And while combined PHY-LINK chips are commercially available, such chips operate on the same ground potential and thus are unsuitable for distributed systems where differences in ground potential may exist. Thus, there is a need for structures for connecting digital devices while isolating them from undesired direct current while also conforming with the trend toward miniaturization of electronic devices.

SUMMARY OF THE INVENTION

The present invention is directed to electronic module packages having a capacitor incorporated within the package for electrically isolating the modules. The resulting package requires less external electronic components than the assemblies currently employed to electrically isolate modules. The present invention is further directed to methods for electrically isolating modules within a package assembly.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a pictorial diagram showing a conventional network in a building.

Figure 2 is a block diagram of conventional networking components according to IEEE 1394.

Figure 3 is a cross-sectional view of a package assembly according to one embodiment of the present invention.

Figure 4 is a cross-sectional view of a package assembly according to another embodiment of the present invention.

Figure 5 is a cross-sectional view of a package assembly according to another embodiment of the present invention.

Figure 6 is a cross-sectional view of a package assembly according to yet another embodiment of the present invention.

Figure 7 is a cross-sectional view of a package assembly according to another embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

As previously mentioned, there is a general trend within the electronics industry towards miniaturization of components such as semiconductor packages. Miniaturization is aided by consolidating various components into a single package. Not only will such a single-package arrangement typically be smaller, but it will ordinarily result in lower manufacturing costs. Embodiments of the present invention include semiconductor package assemblies incorporating a capacitor within the assembly to electrically isolate modules.

Methods and materials for manufacturing semiconductor package assemblies are well-known in the art. Semiconductor devices are typically fabricated on thin wafers of silicon. Several dice are produced on each wafer, with each die representing a single semiconductor device. Each die on a wafer is tested for gross functionality, and sorted according to whether the die passes or fails the gross functionality test. After being sorted according to gross functionality, the wafers are cut using a wafer saw, and the individual die are singulated. The die determined to be non-functional are scrapped. The functional die are packaged and further tested to ensure that each packaged device satisfies a minimum level of performance. Typically, the functional devices are permanently packaged by encapsulating the die in a non-conductive dielectric material. Packaging of the functional devices facilitates handling of the devices and also protects the die from damage during the manufacture of circuits using the packaged devices.

Recently, semiconductor manufacturers have developed a package structure where unpackaged die are mounted directly onto a substrate, for example, a printed circuit board, thus allowing modules to be designed with increased device density. Examples of these types of packages structures include ball grid array (BGA) packages, and other chip scale packages (CSP) having package dimensions that are slightly larger than the dimension of the encapsulated die. The die is mounted onto the substrate and is electrically coupled to conductive traces formed on the substrate by wire bonding the bond pads of the die. Alternatively, the conductive traces and the bond pads may be electrically coupled by using tape automated bonded (TAB) wire instead. The resulting structure is subsequently, partially or entirely, encapsulated to protect the device from damage. External leads, often in the form of solder balls, are then attached to attachment sites on the conductive traces so that the integrated circuit fabricated on the die may be electrically contacted through the external leads.

Following packaging, the device is typically mounted onto a printed circuit board (PCB) as a component in a larger electronic system. Conductive pads on the PCB are positioned to correspond to the location of the external leads of the packaged device. The packaged device is positioned accordingly onto the conductive pads and subjected to a reflow process at an elevated temperature in order to solder the packaged device to the PCB. In the case of a BGA type package, the solder is provided by the solder balls of the completed package.

Figure 3 illustrates an example of a package assembly 300 according to one embodiment of the present invention. A first electronic module 304 and a second electronic module 305 are attached to a substrate 302. The first and second modules are communicatively coupled by metallic traces (not shown) on the substrate that have capacitors in series to prevent direct current from flowing between the modules. A capacitor is formed within the package by conductively coupling the ground plane of the first electronic module 304 to a first conductive surface 310 below the substrate 302, and the ground plane of the second electronic module 305 conductively coupled to the second conductive surface 312 that is spaced apart from the first conductive surface 310. The first and second conductive surfaces 310, 312 are further separated by a dielectric 314. A resistor 308 is coupled between the first and second conductive

surfaces 310, 312 by its first and second terminals respectively to allow the conductive surfaces to equilibrate after power is shut off to the modules.

One of ordinary skill in the art would readily appreciate that various suitable materials may be selected for the package assembly. For example, the resistor can be of any size sufficient to store a charge on the conductive surfaces while in operation and allow the conductive surfaces to equilibrate after power is shut off. Typically, however, resistance of approximately one megohm is desirable. Similarly, the dielectric may be any suitable non-conductive material. In addition, the modules 304, 305 may be conductively coupled to the conductive surfaces 310, 312 in a number of ways, such as with wires 306 bonded between the modules 304, 305, and the conductive surfaces 310, 312, or via metallic traces on the substrate. The particular qualities of the electronic components and the means by which they are coupled to other devices as described above are provided as a non-limiting example of a typical embodiment in accordance with the present invention, and are not intended to limit the scope of the present invention.

According to IEEE 1394, the first module 304 is a PHY chip conductively coupled to a serial bus (not shown) in order to send signals to or receive signals from another device on the bus. The PHY chip 304 is further conductively coupled to the ground wire of the serial bus (not shown). The second electronic module 305 is a LINK chip that is communicatively coupled to the PHY chip 304 via a number of capacitors in series (not shown); the communicative coupling transmits signals originating from the serial bus and processed by the PHY chip 304. The LINK chip 305 is further conductively coupled to the chassis of the computer (not shown) in which it is housed. The PHY 304 and LINK 305 chips are each conductively coupled to a first conductive surface 310 and second conductive surface 312, respectively. A capacitor is formed within the package assembly by the first conductive surface 310 being conductively coupled to the serial bus ground wire (not shown) and spaced apart by a dielectric from the second conductive surface 312, which is conductively coupled to the chassis ground 216 of the computer (not shown) and the LINK chip 305. A resistor 308 provides a path to the local chassis ground in the event a charge is coupled to the serial bus ground. In addition, when power is shut off to the PHY and LINK chips 304, 305,

the resistor 308 allows the direct current to flow between the surfaces 310, 312 to normalize any potential differences between the two surfaces while preventing too much direct current from damaging the first 304 and second 305 modules that are conductively coupled to the conductive surfaces. Although the resistor 308 is depicted as external, one skilled in the art would readily appreciate that the resistors in the embodiments discussed herein may be integral to the semiconductor device packages and formed of any suitable material, such as thin resistive film. The particular qualities of the modules and how they are coupled to other devices as described above are provided as a non-limiting example of an embodiment in accordance with the present invention, and are not intended to limit the scope of the present invention.

Figure 4 illustrates a cross sectional view of another embodiment of the present invention where first and second integrated circuits 416, 418 are incorporated within a single module 404 while remaining electrically isolated. Methods and materials for manufacturing a single module having two or more semiconductors are well-known in the art, and will not be described in detail herein. A capacitor is formed by the ground pin (not shown) of the first integrated circuit 416 conductively coupled to the first conductive surface 410 spaced apart from the second integrated circuit 418 conductively coupled by its ground pin (not shown) to the second conductive surface 412 using wires 406 or any other suitable conductive coupling.

Figure 5 illustrates another embodiment of the present invention where the package assembly has electronic modules 504, 505 on separate substrates 502, 503 within the assembly. In this embodiment, a first electronic module 504 is attached to a first substrate 502 and a second electronic module 505 attached to a second substrate 503 are spaced apart by the first and second conductive surfaces 510, 512 and the dielectric 514. As with other embodiments of the invention, the first and second electronic modules 504, 505 are conductively coupled to the first and second conductive surfaces 510, 512 respectively with wire bonds 506 or any other suitable conductive couplings. A dielectric 514 is interposed between the conductive surfaces 510, 512 to prevent direct current from flowing between the conductive surfaces.

Figure 6 illustrates yet another embodiment of the present invention, where the capacitor formed by the first and second conductive surfaces 610, 612 and

dielectric 614 is on the same side of the substrate 602 as the first and second electronic modules 604, 605. The electronic modules 604 605 may also be combined into a single structure as shown in Figure 4.

Figure 7 illustrates another embodiment of the invention where the first and second electronic modules 704, 705 are stacked on the substrate 702, as opposed to both being attached to the substrate as illustrated in, for example, Figures 3 and 6. The electronic modules 704, 705 are attached with adhesive at the bondline 718. Methods and materials for attaching electronic modules with adhesives are well-known in the art, and the details will not be described in detail herein.

From the foregoing it will be appreciated that, although specific embodiments of the invention have been described herein for purposes of illustration, various modifications may be made without deviating from the spirit and scope of the invention. Accordingly, the invention is not limited except as by the appended claims.